

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Peter John McElheny
Application No. : Not yet available
Confirmation No. : Not yet available
Filed : Concurrently herewith
For : PROGRAMMABLE LOGIC DEVICE DESIGN TOOLS
WITH GATE LEAKAGE REDUCTION CAPABILITIES
Group Art Unit :
Examiner :

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

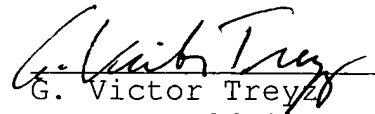
Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, applicant hereby brings the attention of the Examiner to the documents listed on the attached Form PTO-1449 (submitted in duplicate).

A notice in the Official Gazette of August 5, 2003 waived the requirement under 37 C.F.R. § 1.98(a)(2)(i) for submitting a copy of each U.S. patent in Information Disclosure Statements for patent applications filed after June 30, 2003. Accordingly, no copies of cited U.S. patents are enclosed. A

copy of each listed document that is not a U.S. patent is
enclosed herewith.

Respectfully Submitted,

 1/22/04
G. Victor Treyz
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Attorney for Applicants
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	
		Filing Date	Herewith
		First Named Inventor	Peter John McElheny
		Art Unit	
		Examiner Name	
Sheet 1 of 1	Attorney Docket Number	A1167	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		RAFIK S. GUINDI ET AL., "Design Techniques for Gate-Leakage Reduction in CMOS Circuits," 2003 IEEE pp. 61-65	
		VIJAYKRISHNAN NARAYANAN, "Managing Leakage: From Circuits to Software" http://www.cse.psu.edu/~mdl , Comp. Architecture Seminar, UT Austin 2/18/02	
		"Part II Leakage Reduction Techniques", ICCAD 2002 Tutorial; pp 1-50	
		AFSHIN ABDOLLAHI ET AL., "Runtime Mechanisms for Leakage Current Reduction in CMOS VSLI Circuits", ISLPED' 02, August 12-14, 2002	
		JAMES KAO ET AL. "Transistor Sizing Issues and Tool for Multi-Threshold CMOS Technology," DAC 97, Anaheim, CA (c) 1997	
		MOHAB ANIS ET AL., "Dynamic and Leakage Power Reduction in MTCMOS Circuits Using an Automated Efficient Gate Clustering Technique" (undated)	
		B. NIKOLIC, "Advanced Digital Circuits" EE241 Lecture Notes, Spring 2002	
		FEI LI ET AL. "Maximum Current Estimation Considering Power Gating" http://eda.ece.wisc.edu (undated)	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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